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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/866,781 | 05/30/2001 | Daping Chu | 109677 | 5070 |

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
|---|---|
| HU, SHOUXIANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/866,781 | CHU, DAPING |
| | Examiner | Art Unit |
| | Shouxiang Hu | 2811 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-4,6,17-19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,6,17-19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 2-4, 6, 17-19, 21 and 22 are objected to because of the following informalities and/or defects:

Claim 21 recites a plurality of comparators, but fails to clarify their relationships with the recited memory cells, especially regarding whether one comparator is for a single memory cell or for a row of memory cells or for a two dimensional matrix of memory cells.

Claim 22 recite the term of "a signal between" should read as: a voltage between".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2-4, 6, 17-19, 21 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 21 recites the

subject matters that the memory cells are provided at intersections between the recited first and second electrodes, and that the second electrodes are between the first and third electrode; but, according to the original specification, the memory cells are each provided at two intersections, one between the recited first and second electrodes, and the other between the recited second and third electrodes.

In addition, claims 3 and 4 each recite the subject matters of devices that can maintain a constant space between or a constant force stress upon the first and third electrode; but the original specification lacks an adequate description regarding these subject matters, especially regarding how such constant space and/or stress could be absolutely achieved, given that the space and the stress each vary more or less when a voltage is applied to the piezoelectric layer.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2-4, 6, 17-19, 21 and 22, insoafar as being in compliance with 35 U.S.C.112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 102(b) as being anticipated by Adachi (JP 4-38866; 02/1992; of record).

Adachi discloses a device structure (see Figs. 3-5, 7, 8 and 12; also see the English abstract), comprising a plurality of memory elements, each having: a piezoelectric layer and a ferroelectric layer (20 and 23); a plurality of second electrode (the common electrode 31); a plurality of first electrodes (the bottom electrode 26; input/output) and a plurality of third electrodes (the top electrode 21; output/input), wherein the two piezoelectric/ferroelectric layers are naturally clamped, as they are stress-laminated together (see the English abstract); and the device naturally comprises a means that naturally functions as a comparator (as shown in Figs. 3-5 and 12, especially see Figs. 4 and 12) having a pair of inputs for providing an indication of a logic state of the memory device through comparing the phase of a signal across the input and common electrodes with a phase of a signal across the output and common electrode, as the measurement of the polarity of the output current therein (shown in Fig. 12; also see page 16 of the English translation provided by the applicant) naturally involves comparison between voltages of the input voltage (Vin) and the output voltage (Vout). And, it is also noted that the device of Adachi naturally comprises a plurality of such comparators in the sense that each of the memory cells therein has its own circuit arrangements for providing its corresponding first and second inputs for the naturally involved comparison of Vin and Vout during the measurement of its output current polarity.

Regarding claims 6 and 17-19, the input and output electrodes in Adachi are parallel to each other and perpendicular to the common electrode.

Regarding claim 20, the piezoelectric layer and ferroelectric layer in Adachi are naturally mechanically and electrically coupled together, as they are stress-laminated together.

### *Response to Arguments*

6. Applicant's arguments filed on 2-28-2005 have been fully considered but they are not persuasive.

Applicant's main arguments include: Adachi does not disclose the recited comparator. In response, it is noted that the device of Adachi naturally comprises a means that naturally functions as a comparator, as Adachi requires the measurement of the polarity of the output current of each memory cell. And, as shown in Fig. 12 in Adachi, such measurement naturally involves the comparison between voltages of the input voltage (Vin) and the output voltage (Vout), as the measured polarity has to use the input voltage (Vin) as a reference so as to decide the output polarity with respective to the input voltage (Vin, i.e., the reading voltage).

And, it is also noted that the device of Adachi naturally comprises a plurality of such comparators in the sense that each of the memory cells therein has its own circuit arrangements for providing its corresponding first and second inputs for the naturally involved comparison of Vin and Vout during the measurement of its output current polarity.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 28, 2005

**SHOUXIANG HU**
**PRIMARY EXAMINER**